PROCESSOR DESIGN FOR EXTENDED-PRECISION ARITHMETIC

ABSTRACT

A processor for performing a multiply-add instruction on a multiplicand A, a multiplier B, and an addend C, to calculate a result D. The operands are double-precision floating point numbers and the result D is a canonical-form extended-precision floating point number having a high order component and a low order component. The processor is a fused multiply-add processor with a multiplier, an adder, a normalizer and a rounder. The post-adder data path, the normalizer and the rounder each have a data width sufficient to represent post-adder intermediate results to permit the high and low order words of a correctly-rounded result D to be computed. The mantissas of the extended-precision result D are provided such that the high order word mantissa is stored to double precision registers.